IN THE CLAIMS:

This listing of claims replaces all prior listings:

1. (Currently amended) An apparatus, said apparatus comprising:

a semiconductor device including a central processing unit (CPU) and a read control circuit (RCC);

a data-rewritable nonvolatile memory communicatively coupled to the CPU that includes a plurality of data blocks with each data block including a plurality of data pages,

wherein,

at least two boot program instructions are stored in a predetermined number of data blocks in parallel in the data-rewritable nonvolatile memory, the predetermined number being less than the total number of data blocks,

block state information indicating that a data block is faulty or not faulty is stored in a leading data page of each of the data blocks storing boot program instructions,

the CPU is configured, in part, to specify to the RCC a read position for reading out the boot program instruction from a data block in the data-rewritable nonvolatile memory at a starting time[[,]]; and

the RCC is configured to (a) determine whether [[the]] a first respective data block is faulty or not according to the block state information, (b) output [[the]] first data to the CPU when the first respective data block is determined as not faulty, and (c) read, when the first respective data block is determined as faulty, second data from [[the]] a second respective data block and output the ~~said~~ second data to the CPU when the ~~said~~ second respective data block is determined as not faulty, and

the RCC prevents the CPU from accessing the data-rewritable ~~non-volatile~~ nonvolatile memory while the RCC determines which of the respective data blocks ~~block~~ to output to the CPU.

2. (currently amended) The apparatus of claim 1, wherein the ~~read control circuit~~ RCC is configured to determine whether a data block is faulty or not faulty at least according to an error correction code contained in [[the]] data read out from the data-rewritable nonvolatile memory.

3. (currently amended) The apparatus of claim 2, wherein the RCC corrects the data and supplies the ~~said~~ data to the CPU when the ~~said~~ RCC determines that the data is correctable according to the error correction code but otherwise determines that the data block is faulty when it determines that the data is uncorrectable data.

4. (currently amended) The apparatus of claim 1, wherein the RCC is configured to determine that a data block is faulty or not faulty at least according to the block state information contained in [[the]] data read out from the data-rewritable nonvolatile memory.

5. (currently amended) The apparatus of claim 4, wherein the RCC determines that the data block is faulty when the block state information does not show a predetermined value.

6. (cancelled)

7. (previously presented) The apparatus of claim 1, wherein the data-rewritable nonvolatile memory is a NAND type flash memory.

8. (cancelled)